Plastic Medium-Power Complementary Silicon Transistors

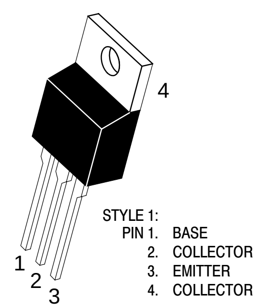
. . . designed for general–purpose amplifier and low–speed switching applications.

- High DC Current Gain — h_{FE} = 2500 (Typ) @ I_C = 1.0 Adc
- Collector–Emitter Sustaining Voltage — @ 30 mAdc
  $V_{CEO(sus)}$ = 60 Vdc (Min) — TIP110, TIP115
  = 80 Vdc (Min) — TIP111, TIP116
  = 100 Vdc (Min) — TIP112, TIP117
- Low Collector–Emitter Saturation Voltage — $V_{CE(sat)}$ = 2.5 Vdc (Max) @ I_C = 2.0 Adc
- Monolithic Construction with Built–in Base–Emitter Shunt Resistors
- TO–220AB Compact Package

NPN
TIP110
TIP111*
TIP112*
PNP
TIP115
TIP116*
TIP117*

*ON Semiconductor Preferred Device

DARLINGTON
2 AMPERE
COMPLEMENTARY SILICON
POWER TRANSISTORS
60–80–100 VOLTS
50 WATTS



CASE 221A–09
TO–220AB

*MAXIMUM RATINGS

Rating	Symbol	TIP110, TIP115	TIP111, TIP116	TIP112, TIP117	Unit
Collector–Emitter Voltage	V_{CEO}	60	80	100	Vdc
Collector–Base Voltage	V_{CB}	60	80	100	Vdc
Emitter–Base Voltage	V_{EB}		5.0		Vdc
Collector Current — Continuous Peak	I_C		2.0 4.0		Adc
Base Current	I_B		50		mAdc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D		50 0.4		Watts W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D		2.0 0.016		Watts W/°C
Unclamped Inductive Load Energy — Figure 13	E		25		mJ
Operating and Storage Junction	T_J, T_{stg}		–65 to +150		°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.5	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

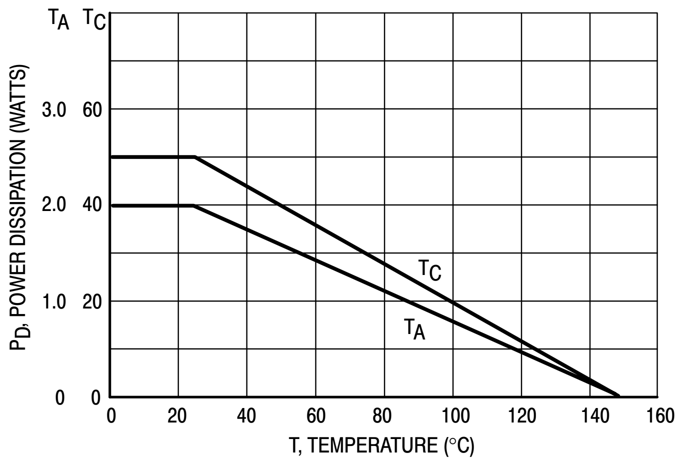


Figure 1. Power Derating

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 30 mAdc, I_B = 0)	TIP110, TIP115		60	—	
	TIP111, TIP116		80	—	
	TIP112, TIP117		100	—	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 30 Vdc, I_B = 0)	TIP110, TIP115		—	2.0	
(V_{CE} = 40 Vdc, I_B = 0)	TIP111, TIP116		—	2.0	
(V_{CE} = 50 Vdc, I_B = 0)	TIP112 ,TIP117		—	2.0	
Collector Cutoff Current		I_{CBO}			mAdc
(V_{CB} = 60 Vdc, I_E = 0)	TIP110, TIP115		—	1.0	
(V_{CB} = 80 Vdc, I_E = 0)	TIP111, TIP116		—	1.0	
(V_{CB} = 100 Vdc, I_E = 0)	TIP112, TIP117		—	1.0	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	—	2.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			—
(I_C = 1.0 Adc, V_{CE} = 4.0 Vdc)			1000	—	
(I_C = 2.0 Adc, V_{CE} = 4.0 Vdc)			500	—	
Collector–Emitter Saturation Voltage (I_C = 2.0 Adc, I_B = 8.0 mAdc)		$V_{CE(sat)}$	—	2.5	Vdc
Base–Emitter On Voltage (I_C = 2.0 Adc, V_{CE} = 4.0 Vdc)		$V_{BE(on)}$	—	2.8	Vdc
DYNAMIC CHARACTERISTICS					
Small–Signal Current Gain (I_C = 0.75 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)		h_{fe}	25	—	—
Output Capacitance		C_{ob}			pF
(V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	TIP115, TIP116, TIP117		—	200	
	TIP110, TIP111, TIP112		—	100	

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

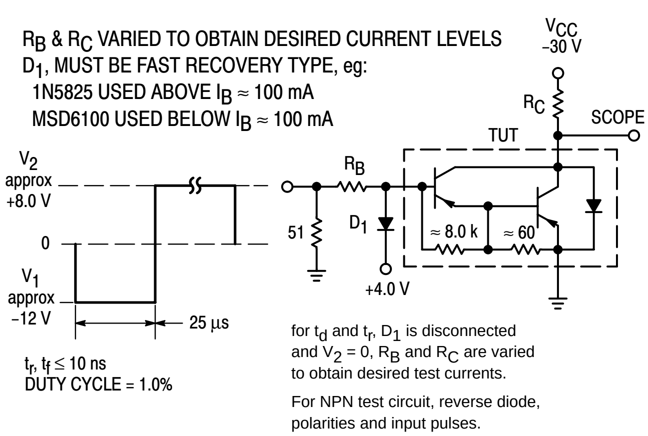


Figure 2. Switching Times Test Circuit

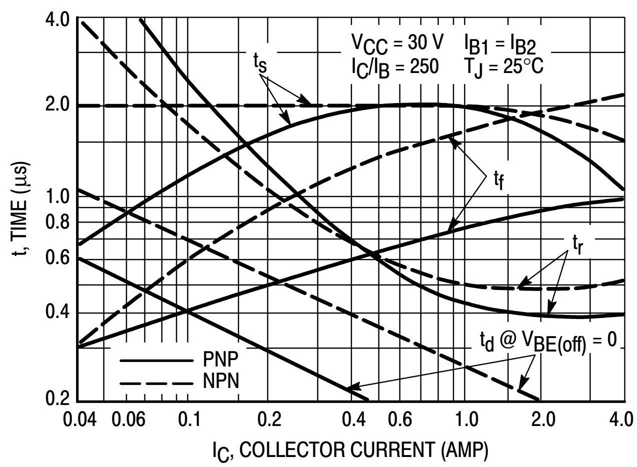


Figure 3. Switching Times

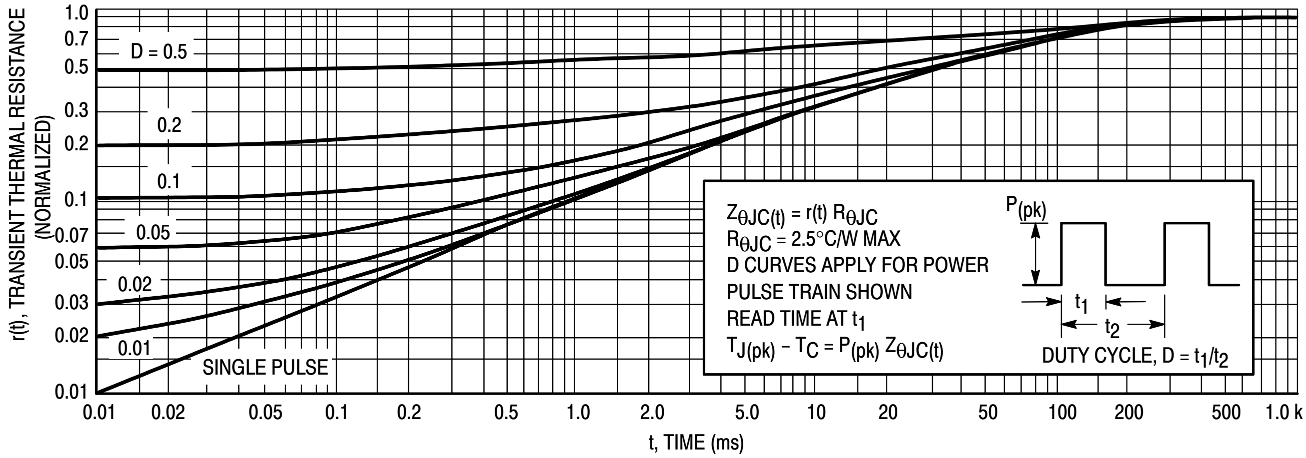


Figure 4. Thermal Response

ACTIVE–REGION SAFE–OPERATING AREA

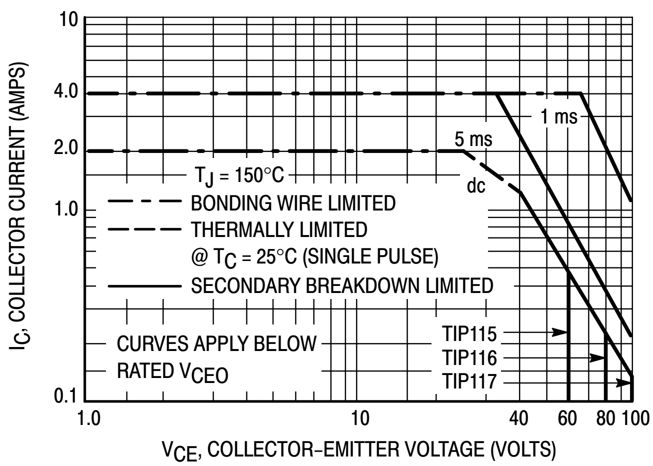


Figure 5. TIP115, 116, 117

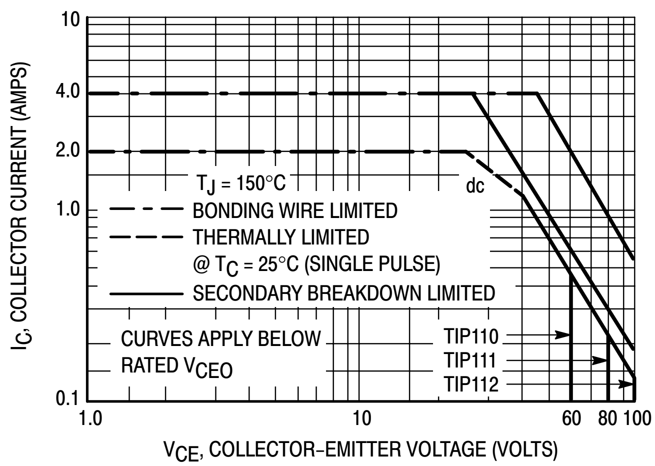


Figure 6. TIP110, 111, 112

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 5 and 6 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

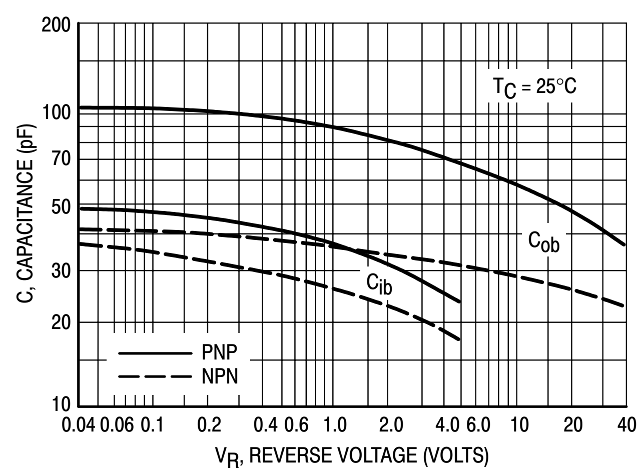


Figure 7. Capacitance

NPN
TIP110, 111, 112

PNP
TIP115, 116, 117

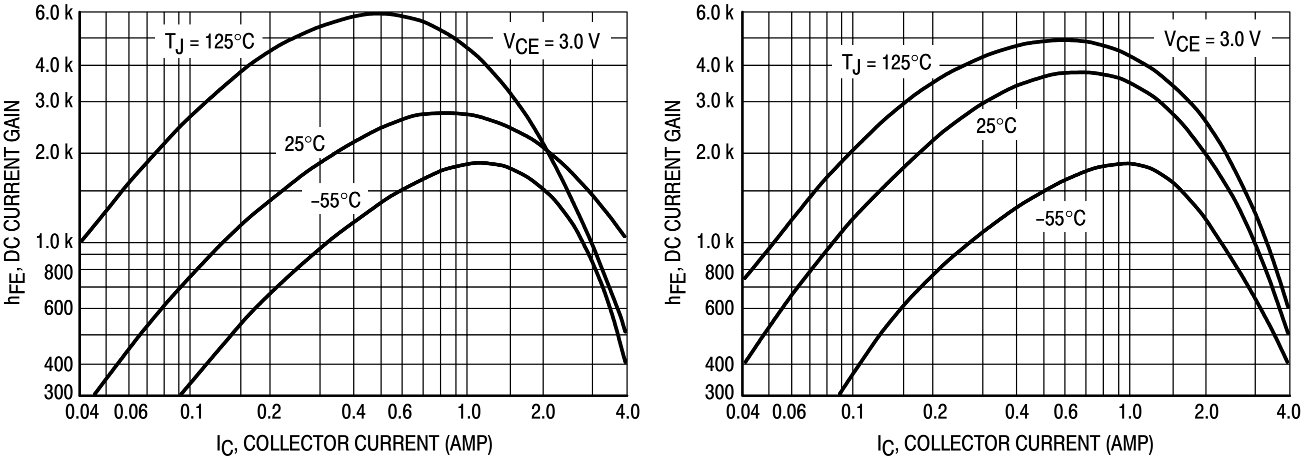


Figure 8. DC Current Gain

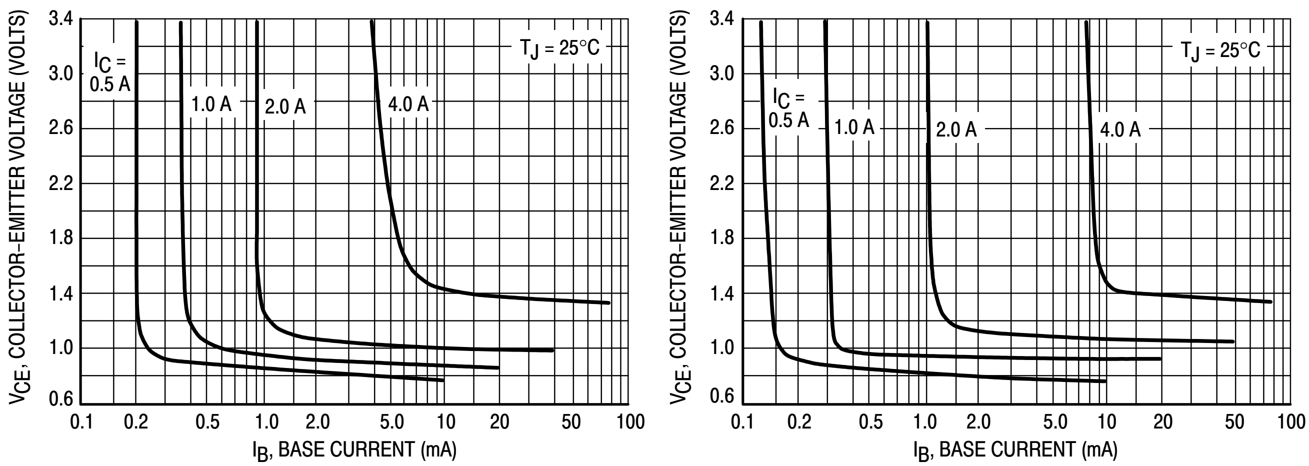


Figure 9. Collector Saturation Region

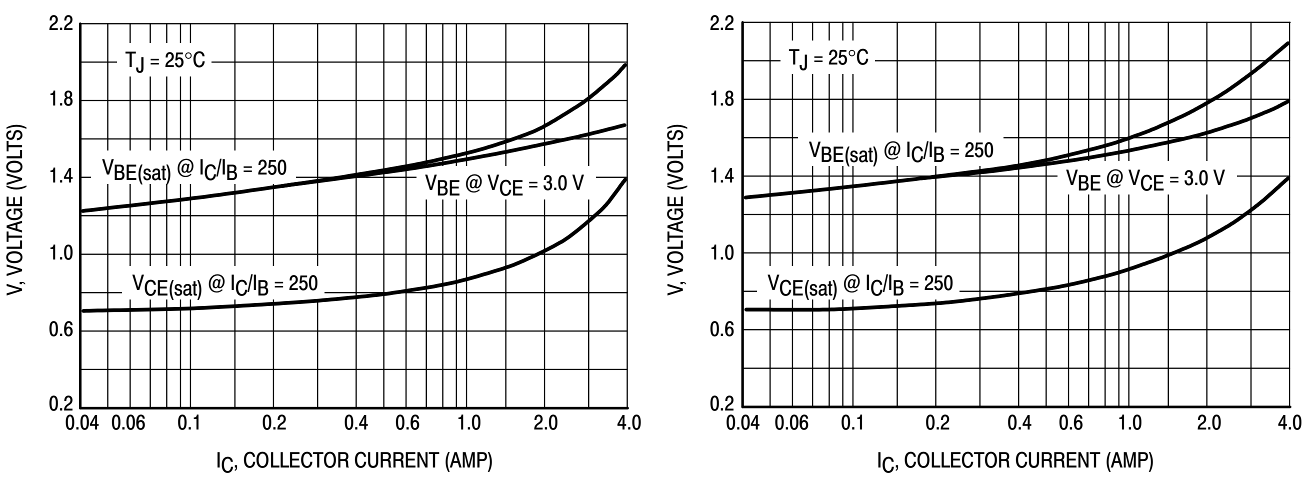


Figure 10. “On” Voltages

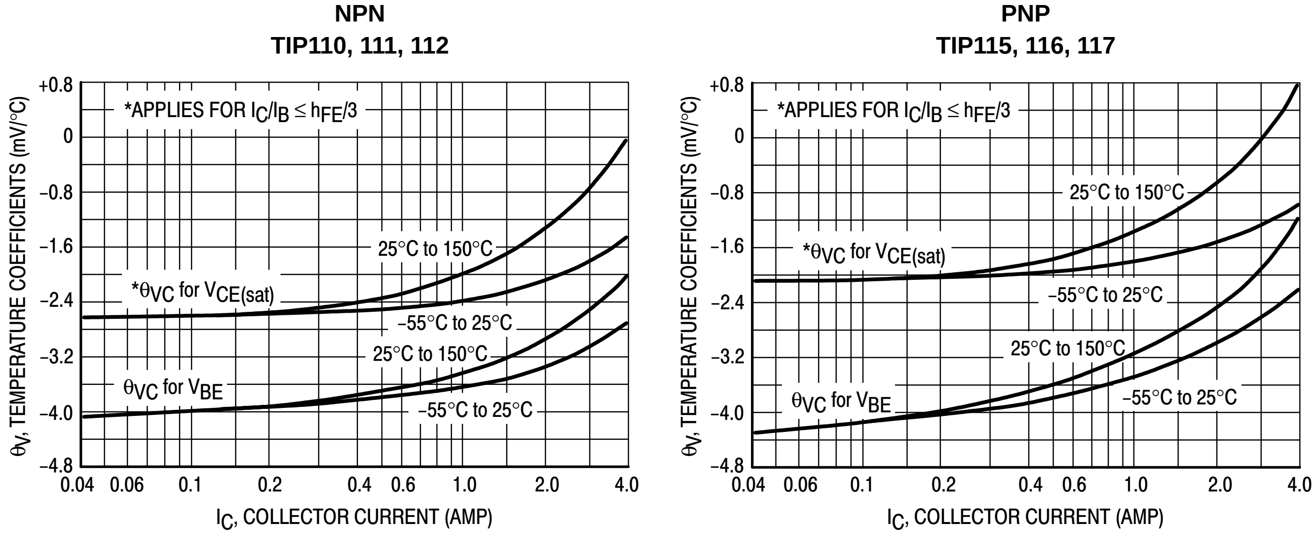


Figure 11. Temperature Coefficients

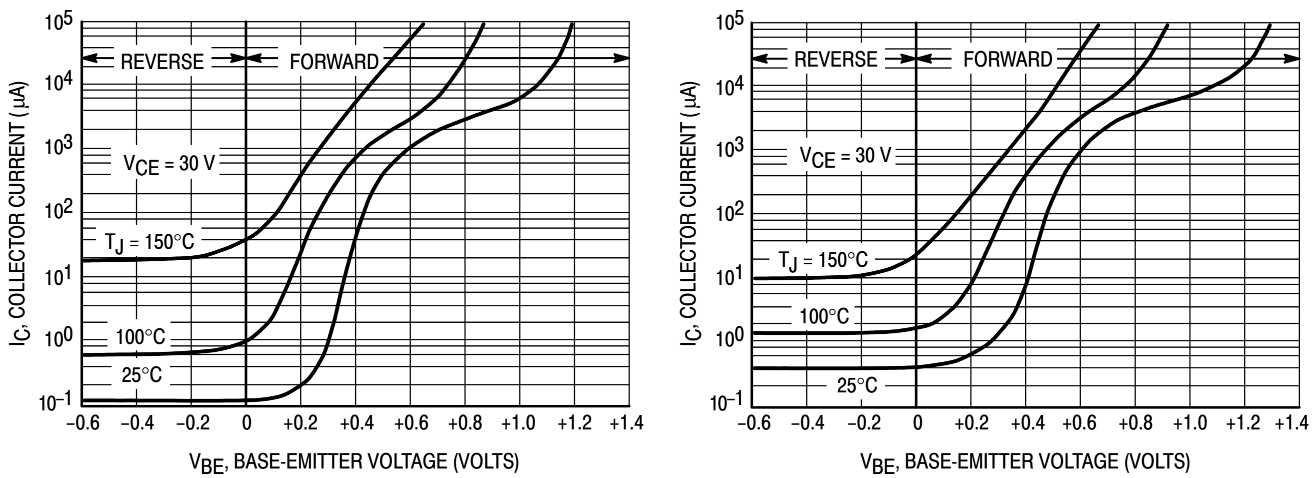
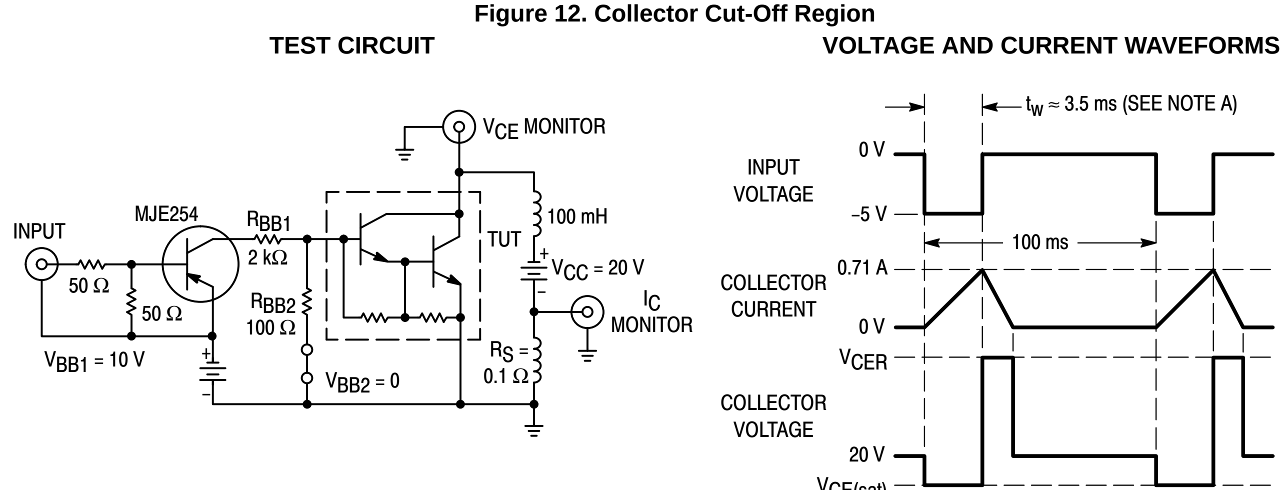


Figure 12. Collector Cut-Off Region



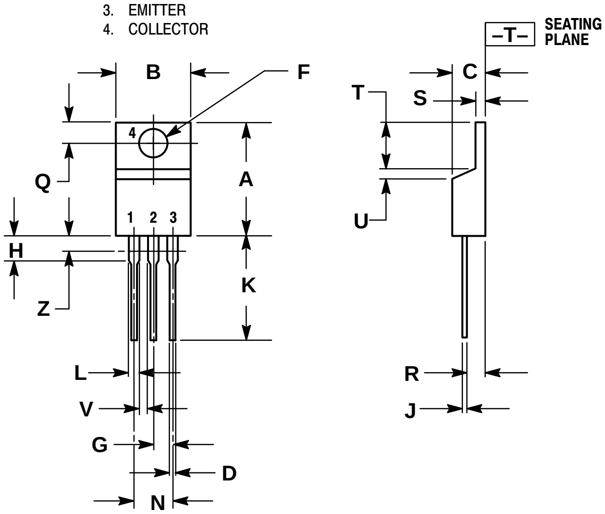
Note A: Input pulse width is increased until I_{CM} = 0.71 A,
NPN test shown; for PNP test
reverse all polarity and use MJE224 driver.

Figure 13. Inductive Load Switching

PACKAGE DIMENSIONS

TO–220AB
CASE 221A–09
ISSUE AA

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

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